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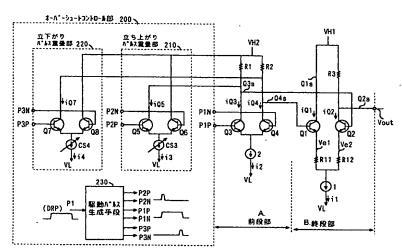
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(54) Title: SEMICONDUCTOR TESTER

(54) 発明の名称: 半導体試験装置



200...OVERSHOOT CONTROL UNIT

220...FALL PULSE SUPERIMPOSING SECTION

210...RISE PULSE SUPERIMPOSING SECTION

230...DRIVE PULSE GENERATING MEANS

A...PRECEDING STAGE

(57) Abstract: A semiconductor tester comprising a driver circuit for generating a predetermined driver waveform without using a coil device. The driver circuit provided in a pin electronics receives a waveform-shaped signal to be supplied to an IC pin of a device under test (DUT) and converts the amplitude to an amplitude of predetermined level. The driver output pulse outputted from the output terminal of the driver and having the converted amplitude is supplied to the IC pin of the DUT. The tester has pulse compensating means for compensating the individual waveforms of the rising and falling edges of the driver output pulse in a predetermined way.

INTERNATIONAL SEARCH REPORT

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A. CLASSIFICATION OF SUBJECT MATTER Int.Cl ⁷ G01R31/28	
According to International Patent Classification (IPC) or to both national classification and IPC	
B. FIELDS SEARCHED	
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Int.Cl ⁷ G01R31/28, H04L25/03	
Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched Jitsuyo Shinan Koho 1922-1996 Jitsuyo Shinan Toroku Koho 1996-2003 Kokai Jitsuyo Shinan Koho 1971-2003 Toroku Jitsuyo Shinan Koho 1994-2003	
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C. DOCUMENTS CONSIDERED TO BE RELEVANT	
Category* Citation of document, with indication, where ap	propriate, of the relevant passages Relevant to claim No.
<pre>X JP 8-242151 A (Hitachi, Ltd.), 17 September, 1996 (17.09.96), Full text; all drawings (Family: none) X JP 4-189051 A (Hitachi, Ltd.), 07 July, 1992 (07.07.92), Full text; all drawings (Family: none)</pre>	
Further documents are listed in the continuation of Box C.	See patent family annex.
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